converts the CRC coded sequence into a code using $1/(1 + D^2)$ as a transfer function. Here, D is the delay operator that provides a delay time equal to the distance between bits. The precoder 103 and reproducing-side postcoders 112 can suppress the decoded error propagation length after Viterbi detection to a definite value. Therefore, the CRC can detect on the reproducing side all error patterns that have been limited to a definite length by the above means. The precoded sequence is supplied through an amplifier 104 to a record head 105 by which it is recorded as magnetic information on a magnetic recording medium 106.--

IN THE CLAIMS

Please add new claims 2-12 as follows:

--2. (New) A digital magnetic recording/reproducing apparatus for recording and reproducing digital information comprising:

a Viterbi detector which decodes a signal sequence obtained by partial response equalization and produces n candidates of a decoded result, the candidates being a best candidate to an nth best candidate and being produced simultaneously by the Viterbi decoder;

an error detector which detects errors in the n candidates; and

an selector which selects from the candidates a candidate having no detected errors as a correct decoded

result and supplies the correct decoded result to a recording decoder;

wherein the Viterbi decoder uses a path memory having a length which is shorter than a length of an error detection block used by the error detector.

3. (New) A digital magnetic recording/reproducing apparatus according to claim 2, wherein the length of the error detection block is selected so that a coding rate after error detection is not less than 8/9.

4. (New) A digital magnetic recording/reproducing apparatus according to claim 2, wherein the error detection block is a CRC (Cyclic Redundancy Check) block.

5. (New) A digital magnetic recording/reproducing apparatus according to claim 2, wherein the Viterbi detector uses an LVA (List Viterbi Algorithm) for signal processing.

6. (New) A digital magnetic recording/reproducing apparatus according to claim 2, further comprising a coder which adds error detection check bits to the signal sequence.

7. (New) A digital magnetic recording/reproducing method for recording and reproducing digital information comprising the steps of:

decoding a signal sequence obtained by partial response equalization and producing n candidates of a decoded result using a Viterbi decoder, the n candidates being a best candidate to an nth best candidate and being produced simultaneously by the Viterbi decoder;

detecting errors in the n candidates; and

selecting a candidate having no detected errors from the n candidates as a correct decoded result.

8. (New) A digital magnetic recording/reproducing method for recording and reproducing digital information comprising the steps of:

decoding a signal sequence obtained by partial response equalization and producing n candidates of a decoded result using a Viterbi decoder, the candidates being a best candidate to an nth best candidate and being produced simultaneously by the Viterbi decoder;

detecting errors in the n candidates; and

selecting from the candidates a candidate having no detected errors as a correct decoded result and supplying the correct decoded result to a recording decoder;

wherein the Viterbi decoder uses a path memory having a length which is shorter than a length of an error detection block used in the error detecting step.

9. (New) A digital magnetic recording/reproducing method according to claim 8, wherein the length of the error

detection block is selected so that a coding rate after error detection is not less than 8/9.

10. (New) A digital magnetic recording/reproducing method according to claim 8, wherein the error detection block is a CRC (Cyclic Redundancy Check) block.

11. (New) A digital magnetic recording/reproducing method according to claim 8, wherein the Viterbi detector uses an LVA (List Viterbi Algorithm) for signal processing.

12. (New) A digital magnetic recording/reproducing method according to claim 8, further comprising the step of adding error detection check bits to the signal sequence.--